which in turn is a continuation of patent application serial no. 07/963,838, filed October 20, 1992, now patent no. 5,297,148, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, now abandoned.--

Please replace the paragraph between page 11, line 23 and page 12, line 5, with the following (a marked up version showing the further amendment is given in the Appendix):

--Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Serial No. 204,175, filed June 8, 1988, by Dr. Eliyahou Harari, now patent no. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," filed on the same day as the present application, Serial No. 07/337,579, filed April 13, 1989, now abandoned, by Sanjay Mehrotra and Dr. Eliyahou Harari. The disclosures of the two applications are hereby incorporated by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.--

In the Claims:

Please replace claim 63 with the following (a marked up version is given in the Appendix):

--63.(Amended) A semiconductor disk device comprising:

a non-volatile, electrically programmable and erasable flash memory including a plurality of sectors, being a unit of erasure for the flash memory;

interface means for exchanging data and addresses with an external system;

an address conversion table for converting sector address information input from the external system into a physical sector number for identifying a sector of the plurality of sectors; and